WHAT IS CLAIMED IS:

1. An integrated circuit having logic blocks comprising

a control unit for performing test and debug operations of said logic blocks of said integrated circuit;

a memory associated with said control unit, said memory holding instructions for said control unit; and

a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed at one or more clock signal rates internal to said integrated circuit.

2. The integrated circuit of claim 1 further comprising

a plurality of probe lines responsive to said control unit for carrying system operation signals at predetermined probe points of said logic blocks, said system operation signals stored in said memory so that said system operation signals are retrieved at one or more clock signal rates internal to said integrated circuit.

3. The integrated circuit of claim 1 further comprising

a unit coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

4. The integrated circuit of claim 1 wherein said scan lines comprise a first string of flip-flop connectors connected between a logic block and the remainder of said integrated circuit proximate said logic block, said flip-flop connectors providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode.

5. The integrated circuit of claim 1 wherein said scan lines comprise a second string of flip-flop connectors between elements of a logic block, said flip-flop connectors providing signal paths between said logic block elements in one mode and carrying test signals and test signal results in a second mode.

6. The integrated circuit of claim 2 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points of said logic blocks in one mode.

7. The integrated circuit of claim 6 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

8. The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying digital state system operation signals.

9. The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals reflective of analog conditions at said predetermined probe points.

10. An integrated circuit comprising

an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing sequential of sets of system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals at predetermined probe points of said integrated circuit;

a memory coupled to said unit and to said interface, said system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit;

whereby said external diagnostics processor can process said captured system operation signals

11. The integrated circuit of claim 10 wherein said unit further comprises trigger logic responsive to said system operation signals for initiating storage of said system operation signals in said memory.

12. The integrated circuit of claim 11 wherein said trigger logic is responsive to said system operation signals for terminating storage of said system operation signals in said memory.

13. The integrated circuit of claim 10 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points in one mode.

14. The integrated circuit of claim 13 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

15. A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of scan lines of said logic blocks, said method comprising

loading said memory with test signals and instructions for said control unit;

loading said scan lines responsive to said control unit with said test signals for said logic blocks at one or more clock signal rates internal to said integrated circuit;

operating said logic blocks at one or more clock signal rates internal to said integrated circuit;

retrieving test signal results from said logic blocks along said scan lines at one or more clock signal rates internal to said integrated circuit,

storing said test signal results in said memory at one or more clock signal rates internal to said integrated circuit; and

processing said stored test results signals in said control unit responsive to said stored instructions in said memory to perform test and debug operations of said logic blocks of said integrated circuit.